In the specification:

Please substitute the following paragraphs for the paragraphs at the indicated locations in the specification as originally filed or most recently amended.

Paragraph [0029]

It will be helpful to an understanding of the nature and scope of the invention from the following description if some definitions of terminology are kept in mind: package is meant to refer to the housing and/or interface between the chip and circuit board; off-chip connection refers to a wirebond pad, C4 bump and the like used to connect the chip to the package (wirebond pad and C4 may sometimes be used synonymously therewith and are intended to encompass all other off-chip connection structures unless the context indicates otherwise); off-chip connection site refers to a potential chip location of an off-chip connection; core cell refers to internal circuits and elements (e.g. digital logic, analog functions, macros and the like) which do not make direct connections off-chip; core cell area refers to the region in which core cells may be placed; I/O cell refers to driver and/or receiver circuitry used to communicate between core cells of the chip and the off-chip connections; I/O cell site or I/O slot refers to locations on a chip in which an I/O cell may be placed under the design rules for the chip; kernel refers to a sub-set of the image generally containing ~~one~~ two or more I/O cell sites and their respective off-chip connection(s) and having power connections independent of other kernels and I/O sites and power busses therefor; corner kernel refers to a kernel placed in the corner of an image and having a shape generally in the shape of an

"L"; edge kernel refers to a kernel that resides only along one edge of an image, size varying with the number of I/O cells therein; filler kernel refers to a kernel used to replace an edge or corner kernel during I/O cell depopulation in accordance with the invention and converts all I/O sites and all or some of the off-chip connections in the replaced kernel to core cell area while other off-chip connections, if any, may be used for power connections tied directly to the internal power grid of the chip.

Paragraph [0033]

A concept exploited by the invention may also be described in connection with Figure 2. Specifically, it will be noted that the two pairs of I/O cell sites 30, 60 at the corners of the chip (or ends of the row of I/O cell sites along each edge of the chip) provide two power connections which are sufficient to provide power to these I/O cell sites as a group, as indicated by ~~65'~~ 65 (indicated by ~~heavy~~ dashed lines) even though power busses would be required. However, since one I/O cell site of each pair is unusable under this particular technique due to both the power busses and the inability to provide signal connection pads 20 and is thus highly inefficient, the invention will use a similar arrangement as a corner kernel which, while different from Figure 2 as will be described below, may be best understood from comparison with corner group 65' of Figure 3. Such a comparison may also be helpful in understanding the concept of a kernel, in general.